REMARKS

Claims 1 and 3-22 were examined, and all claims are rejected. Applicant thanks the Examiner for the withdrawal of the previous prior art rejections.

Claims 1, 3-8, 10-12, 14, 15, 20, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao et al. (U.S. Patent No. 6,275,891) in view of Lowe et al. (U.S. Patent No. 6,173,243) and Selvidge et al. (U.S. Patent No. 5,649,176), claims 9, 17, and 18[1] are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao in view of Lowe, Selvidge, and Ott (U.S. Patent No. 6,400,728), claims 13, 16, and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao in view of Lowe, Selvidge and Stilp (U.S. Patent No. 6,097,336), and claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dao in view of Lowe, Selvidge, Ott, and Stilp. Applicant respectfully traverses these rejections for the reasons set forth below.

The present invention is directed to a signal processing apparatus having a channel pooling signal processor 76 and a digital signal processor (DSP) 72, wherein the channel pooling signal processor 76 performs more computationally intensive signal processing operations than the DSP 72. The channel pooling signal processor 76 has a reconfigurable multiprocessor 66, which has computation units 36 and an interconnect mechanism 32, a test interface 34 for testing the function of the computation units 36, and a microprocessor 74 for managing data flow into and out of the channel pooling signal processor 76. The interconnect mechanism 32 connects the computation units 36, the interface 34, and the microprocessor 74. Each of the computation units 36 has a data sequencer 46 for controlling program execution, a configurable logic unit 44, and a dedicated memory 42.

Dao discloses a processing architecture in which a dedicated, custom-designed hardware accelerator is coupled to a DSP 108 and a DSP memory 110 via a DSP bus 112. The DSP 108 performs less demanding computationally-intensive tasks of pre-processing and post-processing

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[1] Although the rejection heading states that only claim 9 is rejected, it is clear from the remainder of the rejection and the Office Action as a whole that the Examiner intended to reject claims 9, 17, and 18.

data, and allows the hardware accelerator to perform specific processing steps that the DSP 108 is too inefficient to perform. Col. 1, line 61, to col. 2, line 12.

The Examiner has taken the position that since Dao teaches a hardware accelerator and a digital signal processor (DSP), which performs less demanding computationally-intensive tasks (col. 1, line 61 et seq.), and Selvidge discloses that reconfigurable logic devices can find application as hardware accelerators (col. 1, lines 41-42), then the applied references suggest the claimed channel pooling signal processor. Applicant respectfully disagrees. As claimed, and as shown in Figs. 2-5, the channel pooling signal processor 76 includes a reconfigurable multiprocessor 66 having computation units 36 and an interconnect mechanism 32, a test interface 34, and a microprocessor 74. Each computation unit 36 has a data sequencer 46 for controlling program execution, a configurable logic unit 44, and a dedicated memory 42. While Dao may disclose a hardware accelerator, and Selvidge may disclose a reconfigurable logic device finding application as a hardware accelerator, they certainly don't suggest the detailed channel pooling processor as claimed.

The Examiner asserts on page 3 of the Office Action that Dao's hardware accelerator includes a memory, means for controlling memory transfers, additional memories, additional buses, and interfaces between the hardware accelerator and the DSP, and that these elements are computation units. Applicant respectfully disagrees. A computation unit is a unit that computes; memories, buses and interfaces do not compute. Also, the additional memories and additional buses are interfaces between the hardware accelerator and the DSP (col. 2, lines 13-16), and thus do not form part of the hardware accelerator. Further, Dao does not disclose that the hardware accelerator includes a means for controlling memory transfers; Dao merely discloses that "[i]f the hardware accelerator includes its own memory buffer, then direct memory transfers may be used to move data across bus 112;" this statement does not mean that a means for controlling memory transfers is located within the hardware accelerator. Thus the claims are patentable over the applied references for this additional reason.

In an attempt to make up for Dao's and Selvidge's lack of a disclosure of a test interface, the Examiner applies Lowe. While Lowe may disclose a means for testing system functionality (col. 1, lines 28-29), Lowe does not teach or suggest a test interface being in a channel pooling signal processor. Lowe's means for testing is for testing the system functionality as a whole, whereas the claimed test interface is located within and is dedicated to testing internal states of the channel pooling signal processor, including testing the function of the computation units. Thus the claims are patentable over the applied references for this additional reason.

New dependent claims 25-28, which find support in the specification at, for example, page 7, first full paragraph, further recite that the test interface tests the computation units for functionality and reliability while maintaining status and operating modes of all channels that are not being tested in an unchanged state. Since the applied references do not suggest the claimed test interface, it necessarily follows that the applied references also do not suggest this further feature of claims 25-28.

Dependent claims 4 and 5 recite that the computation units are heterogeneous and homogeneous, respectively. There is no suggestion in the applied references of such computation units. The Examiner's only comment regarding these features is "the combination is capable of receiving multiple data streams as shown in Fig. 2 of Dao." (Office Action, page 4, third paragraph.) Dao's Fig. 2 appears to show multiple accelerators and DSPs. Even assuming that the accelerators were the channel pooling signal processors and included computation units, there is no disclosure or suggestion in Dao as to whether the computation units are homogeneous or heterogeneous. Thus claims 4 and 5 are patentable over the applied references for this additional reason.

Dependent claim 7 further requires "configuring a configurable logic unit in said computation unit in accordance with a standard." As can be gleaned from the disclosure, examples of a standard include, but are not limited to, CDMA (code division multiple access) and TDMA (time division multiple access). None of the references applied against claim 7 suggest such a feature, and thus claim 7 is patentable over the applied references for this additional reason.

Finally, new claims 23-36 have been added. New claims 23 and 24 are based on claims 1 and 9, respectively, but include "means for" language. Claims 25-28 are discussed above. Support for new claims 29-32 may be found, for example, in Fig. 5 and the corresponding disclosure, and support for new claims 33-36 may be found in the specification, for example, at page 9, lines 8-13, and Fig. 6. No new matter has been added.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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